Model-based Engineering for Massively Parallel System Design

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DaRT project
Software and hardware co-design for data-intensive embedded systems
Dealing with parallelism and regularity in data-intensive applications

Challenges
Challenges (2)

Finding best implementations for data-intensive applications

Mono-processor architecture

Multi-processor architecture
Proposition Gaspard2 framework
Graphical Array specification for PARallel distributed computing

Design reuse: boosting developer's productivity...
Outline

- MPSoC co-modeling with Marte profile
- Model refinements
- Analysis, simulation and synthesis
MPSoC co-modeling

Marte/UML standard profile
OMG Marte standard profile

Modeling and Analysis of Real-Time Embedded systems (www.omg-marte.org)
Downscaler: main application

Modeling with GCM (General Component Modeling) concepts
Downscaler: HF task

Data-parallel task modeling with RSM concepts

Applied stereotypes:

- FlowPort (from MARTE::MARTE_Foundations::GCM)
  - isAtomic: Boolean [1..1] = false
  - isConjugated: Boolean [1..1] = false
  - direction: DirectionKind [0..1] = in

- Shaped (from MARTE::MARTE_Annexes::RSM)
  - shape: ShapeSpecification [1..1] = {352, 288}

- Tiler (from MARTE::MARTE_Annexes::RSM)
  - origin: IntegerVector [0..1] = {0, 0}
  - paving: IntegerMatrix [0..1] = {{8,0}, {0,1}}
  - fitting: IntegerMatrix [0..1] = {{1,0}}
  - tiler: TilerSpecification [0..1] = null

- Shaped (from MARTE::MARTE_Annexes::RSM)
  - shape: ShapeSpecification [1..1] = {44, 288}
Hardware architecture model

Shared memory multiprocessor architecture
IP instanciation

- Software
  - FFT, DCT, Convolution, FIR
- Hardware
  - Processor, cache, DMAC crossbar
- Energy
  - Processor, cache, DMAC crossbar

GaspardLib
Instanciating HF component in C

**Instanciation**

- **HFil2Block**
  - `in_hf: unsigned int`
  - `out_hf: unsigned int`

- **VHFilter**
  - `vhin`
  - `vhout`

- **softwareIP**
  - `in_h: unsigned int [1]`
  - `out_h: unsigned int [1]`

**IP definition**

- **HFil-C**

- **CodeFile**
  - `sourceFilePath = Software/Filter/hfil.cc`

- **HFil-CodeFile**

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**SoftwareIP** (from deployment)
- entryName: String [1..1] = h_fil
- language: String [1..1] = C
- parameters: Port [0..*] = [hhin, hhout]
- characteristics: Property [0..*] = [executionTime_hf]
- specializations: Property [0..*] = []
Instanciation of cache in systemC

- **HwCache**
  - structure = Direct mapped
  - writePolicy = WriteThrough

- **Cache**
  - cache_slave
  - cache_initiator

- **virtualIP**
  - vcs
  - vcm

- **hardwareIP, hwCache**
  - in_port
  - initiator_port

- **Cache-PA**

- **CodeFile**
  - compilationDirective = -O3 -DNDEBUG -g -march=i686
  - sourceFilePath = Hardware/PVT-PA/Cache/cache.cc
  - headerFilePath = Hardware/PVT-PA/Cache/cache.h
Model refinements

Model transformations for multi-target compilation
Generating static schedulings

Marte model of distribution

Set of mapping constraints of data-parallel tasks on MPSoC

Nested loops parameterized by processor and task IDs

ClooG tool
Implementation w.r.t. MDE

Implementation of transformations with QVTO in Eclipse
Analysis, simulation and synthesis
Experiments with SystemC

Time and energy according to number of processors and cache sizes
Experiments with VHDL

Example of hardware accelerators generated automatically in Gaspard2
Typical case studies

Module of an Anti-collision radar detection system

- Collab with IEMN (a French nanotechnology lab)
- Modeling and VHDL code generation with Gaspard2
- Synthesis via Xilinx tools
- Implemented on Xilinx Virtex II-Pro XC2VP30 FPGA

H.263 video codec

- Intra part of the codec (regular computation part)
- Modeling and SystemC/VHL code generation
- Exploration from 4 to 16 processors in SystemC

Simulation of electromagnetical phenomena

- Collab with L2EP (a French physics lab)
- Modeling of matrix-based algorithms and OpenMP Fortran code generation
- Exploration of execution efficiency w.r.t. Different algorithms
Conclusion

• **A model-driven engineering framework**
  • High-level modeling with the OMG Marte profile
  • Fast compilation towards different target technologies
  • DSE of data-intensive embedded systems on MPSoCs
  • Increase of designer's productivity

• **On-going development...**
  • Usability and comfort: extension of GaspardLib and GUI
  • Traceability in model transformations for debug and DSE
  • State machines for reconfigurable system design
Gaspard2 framework
http://www.gaspard2.org